Fault-Tolerant Flash ADC Architecture for Edge IOT devices

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*of*

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# 📑 **Index**

1. **Introduction** **- 3**  
     1.1 Background: ADCs in IoT and Edge Devices  
     1.2 Motivation for Low-Bit Flash ADCs  
     1.3 Problem Statement: Need for Speed + Fault Detection  
     1.4 Project Objective: 3-bit Flash ADC with Fault-Detection in Cadence Virtuoso
2. **Literature Review / Application Survey**  **- 4**  
     2.1 ADC Roles and Requirements in IoT  
     2.2 Successive Approximation Register   
     2.3 Sigma-Delta (ΣΔ) ADCs (high precision, low bandwidth)  
     2.4 Flash ADCs and Their Use Cases (ultra-fast, low-bit)  
     2.5 Other Architectures (Pipeline, Integrating)  
     2.6 Comparative Analysis of ADCs for IoT  
     2.7 Application Domains  
      • Wearables and Health Monitoring  
      • Industrial and Medical Precision  
      • High-Speed Event Detection  
      • Embedded MCU/SoC Integration  
     2.8 Justification for This Work
3. **Proposed Design: 3-bit Flash ADC - 7**  3.1 Why 3-bit Resolution for IoT Applications  
     3.2 Design Advantages: Simplicity, Speed, and Fault Tolerance  
     3.3 System-Level Overview of the Flash ADC
4. **Block Diagram and Functional Description**  **- 8**  
     4.1 Resistor Ladder Network  
     4.2 Comparator Array (7 Comparators for 3-bit ADC)  
     4.3 Thermometer-to-Binary Encoder  
     4.4 Fault Detection and Warning Block  
     4.5 Digital Output (N-bit Code)
5. **Circuit Diagram - 9**
6. **References - 11**

# **1. Introduction**

### **1.1 Background: ADCs in IoT and Edge Devices**

The Internet of Things (IoT) has created a strong demand for low-power, reliable data converters that can operate efficiently at the edge. Since sensors produce analog signals, an Analog-to-Digital Converter (ADC) is the critical interface to digital processing units.

### **1.2 Motivation for Low-Bit Flash ADCs**

While most IoT nodes use medium-resolution ADCs, certain tasks demand immediate event detection or threshold monitoring. In such cases, high-speed conversion is more important than high resolution. Flash ADCs are ideal for this scenario because of their near-instantaneous conversion, especially when implemented at low resolution (3–4 bits).

### **1.3 Problem Statement: Need for Speed + Fault Detection**

In edge environments, devices operate under varying conditions: supply noise, temperature changes, and reference voltage instability. Conventional Flash ADCs can fail under reference drift, leading to incorrect digital codes. A solution is required that balances speed, low power, and robustness against reference faults.

### **1.4 Project Objective: 3-bit Flash ADC with Fault Detection in Cadence Virtuoso**

This project implements a 3-bit Flash ADC in Cadence Virtuoso, built entirely with analog blocks (resistor ladder, comparators, encoder). Additionally, a fault-detection block monitors the reference voltage (Vref) and raises an error flag when instability is detected.

# **2. Literature Review / Application Survey**

## **2.1 ADC Roles and Requirements in IoT**

IoT edge devices interface with diverse sensors and must convert analog signals into digital form under strict resource constraints. Key requirements:

* Ultra-low power consumption (battery or harvested energy).
* Sufficient resolution and accuracy depending on the sensor type.
* Sampling rate and latency tuned to the application.
* Low cost and compact silicon area.
* Seamless integration with SoCs and microcontrollers.

General trends in IoT:

* Low-power sensing → SAR ADCs dominate.
* High-precision sensing → ΣΔ ADCs are preferred.
* High-speed or transient capture → Flash or pipeline ADCs.

## **2.2 Successive Approximation Register (SAR) ADCs**

* Resolution: Medium (8–12 bits).
* Power: Low to very low, suitable for battery IoT nodes.
* Speed: Moderate, sampling rates in the hundreds of kS/s to a few MS/s.
* Use cases: General-purpose IoT sensing (temperature, humidity, pressure, etc.).
* Strength: Balanced trade-off between resolution, speed, and power.
* Limitation: Cannot handle *instantaneous high-speed events*.

## **2.3 Sigma-Delta (ΣΔ) ADCs**

* Resolution: Very high (16–24 bits).
* Power: Moderate, depends on oversampling ratio.
* Bandwidth: Low, unsuitable for fast changes.
* Use cases: Medical wearables, precision industrial sensing, environmental monitoring.
* Strength: Noise shaping, excellent accuracy.
* Limitation: Slow — not usable for rapid signal edge detection.

## **2.4 Flash ADCs and Their Use Cases**

* Architecture: Resistor ladder + 2ⁿ−1 comparators + encoder.
* Resolution: Limited (≤3–4 bits practical for low-power).
* Speed: Fastest ADC architecture — one comparator delay only.
* Power: High at large resolutions, but *manageable* for very low bit designs (3-bit in this work).
* Use cases: Event detection, digitization of transients, embedded monitoring channels.
* Strength: Zero-latency, ideal for capturing sudden changes.
* Limitation: Scaling to higher resolution is power-hungry and area-inefficient.

## **2.5 Other Architectures (Pipeline, Integrating)**

* Pipeline ADCs: Used in high-throughput systems (wireless base stations, image sensors). Too complex and power-intensive for IoT nodes.
* Integrating ADCs (dual slope): Excellent noise immunity, widely used in digital multimeters. However, very slow, unsuitable for real-time IoT edge processing.

## **2.6 Comparative Analysis of ADCs for IoT**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **ADC Type** | **Resolution** | **Speed** | **Power** | **Suitability for IoT Edge** | **Remarks** |
| **SAR** | Medium (8–12b) | Moderate | Low | Excellent for general sensing | Balanced, most common in IoT nodes. |
| **ΣΔ** | High (16–24b) | Low | Medium | Best for precision sensing | Not suitable for high-speed detection. |
| **Flash** | Low (3–4b) | Very High | High (but reduced at low bit count) | Suitable for event detection | Ideal for fast edge monitoring in low-resolution cases. |
| **Pipeline** | Medium–High | High | High | Not suitable | Complexity and power overhead. |
| **Integrating** | Medium | Very Low | Very Low | Not suitable for real-time | Too slow for edge IoT. |

## **2.7 Application Domains**

* Wearables/Health Monitoring: Flash ADCs can act as auxiliary blocks to detect fast biosignal thresholds (arrhythmia, sudden motion events).
* Industrial/Medical Precision: ΣΔ or SAR dominate, but Flash ADCs can monitor for anomalies requiring instant response.
* High-Speed Event Detection: Flash ADCs are unmatched for capturing short-lived signals (glitches, spikes, rapid transitions).
* Embedded MCUs/SoCs: Low-bit Flash ADCs are often integrated for internal monitoring (battery health, reference stability).

## **2.8 Justification for This Work**

Although SAR and ΣΔ ADCs are more widely deployed in IoT edge devices, this project deliberately implements a 3-bit Flash ADC because:

1. Speed Demonstration: Flash ADC is the fastest architecture — useful to explore event-driven or trigger-based IoT circuits.
2. Educational Scope: A 3-bit Flash design is compact, making it feasible to implement and simulate in 180 nm CMOS without excessive area/power.
3. Testing Fault-Tolerant Ideas: Adding a fault-detection block (e.g., monitoring reference voltage stability) is easier to integrate with Flash due to its simple structure.
4. Proof-of-Concept: While SAR or hybrid ADCs may be more practical in IoT, starting with Flash validates the comparator and encoder design, building a foundation for more advanced future architectures.

# **3. Proposed Design: 3-bit Flash ADC**

### **3.1 Why 3-bit Resolution for IoT Applications**

* Keeps comparator count low (7 comparators).
* Provides fast response with minimal silicon area.
* Enough resolution for threshold-based IoT sensing and edge-triggered applications.

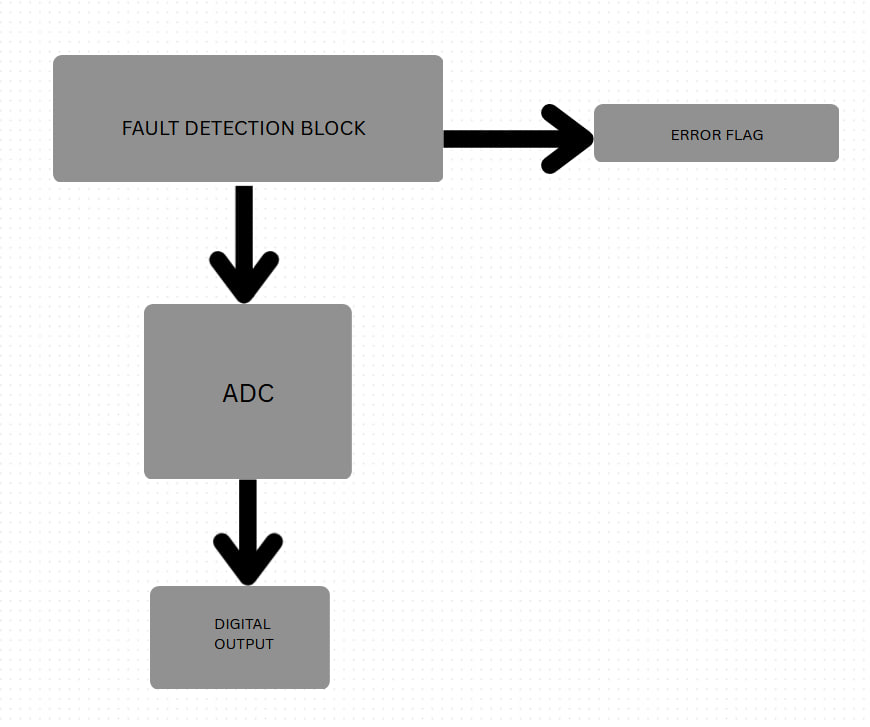
### **3.2 Design Advantages: Simplicity, Speed, and Fault Tolerance**

* Simplicity: Straightforward ladder + comparator + encoder structure.
* Speed: Flash topology ensures conversion in one step.
* Fault Tolerance: Added reference monitoring enhances robustness against supply noise or drift.

### **3.3 System-Level Overview**

* Input analog voltage (Vin) is compared against reference ladder points.
* Comparator outputs form thermometer code.
* Encoder block converts thermometer to binary.
* Fault detection monitors Vref and generates an error flag if instability occurs.

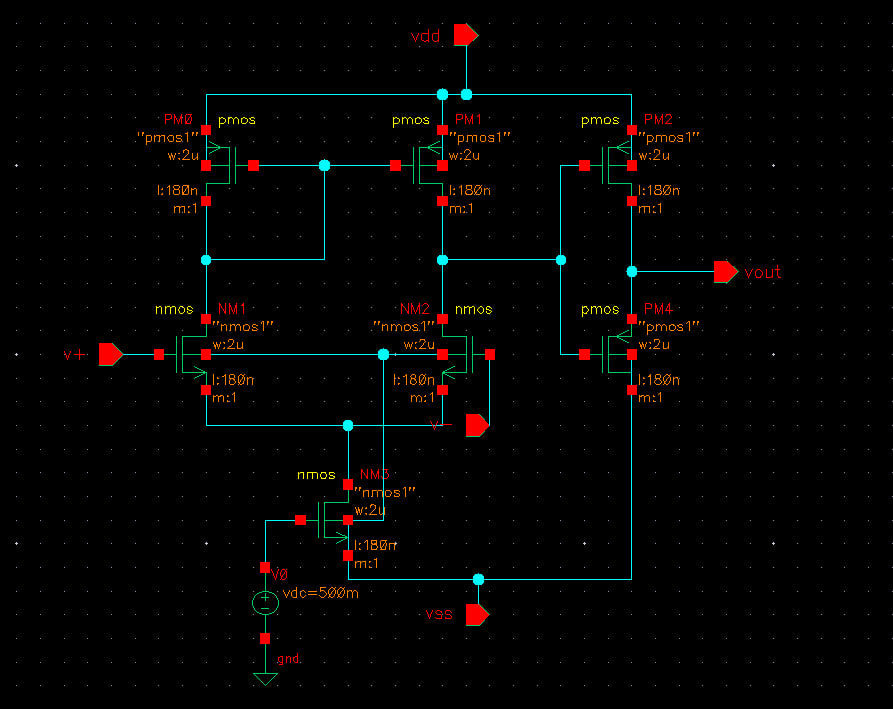
# **4. Block Diagram**



*Figure 4.1*

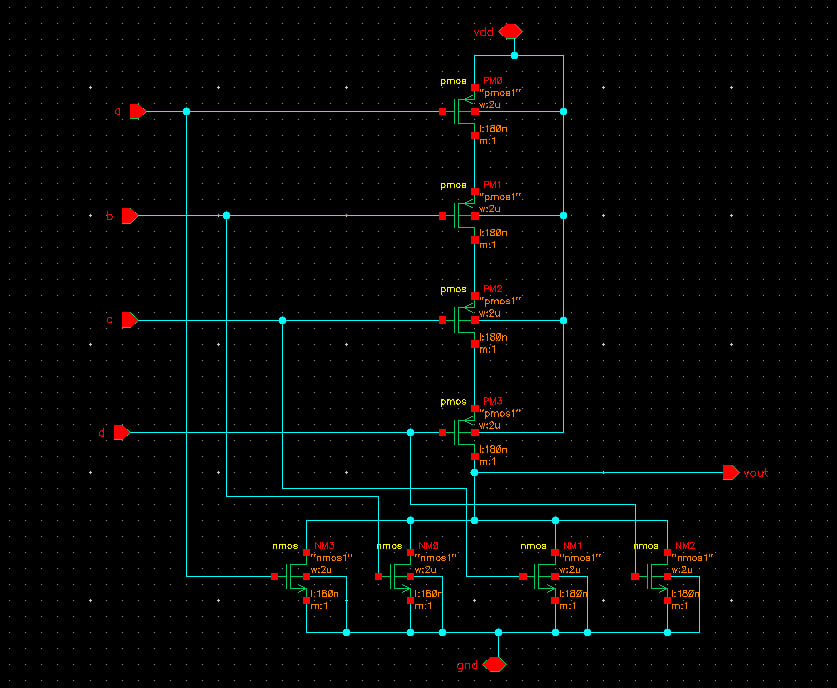
# **5. Circuit diagram**

1. **Comparator**



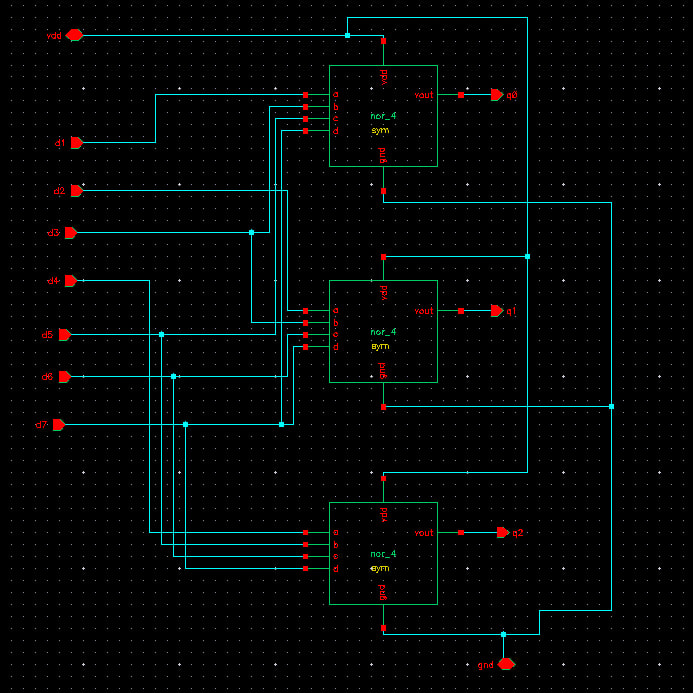
*Figure 5.1*

**2. 4 input NOR Gate**



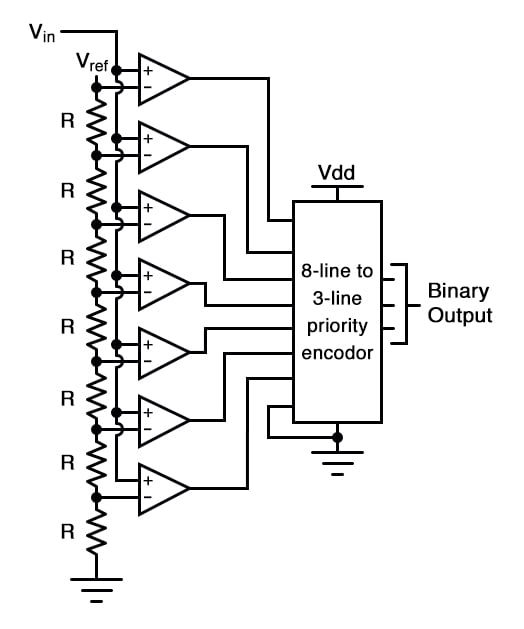
*Figure 5.2*

**3. Priority encoder**



*Figure 5.3*

**4. 3 bit Flash ADC**



*Figure 5.4*

**6. References**

1. P. Harpe, K. A. A. Makinwa, and A. Baschirotto, Eds., \*Hybrid ADCs, Smart Sensors for the IoT, and Sub-1V & Advanced Node Analog Circuit Design\*. Cham: Springer, 2018. doi: 10.1007/978-3-319-61285-0..
2. N. H. Patel, “Power efficient 4-bit flash ADC using Cadence Virtuoso,”

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